UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,243	09/03/2003	Woo-Hyun Kim	041993-5232	2820

9629 7590 12/14/2005

MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
VU, PHU	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/653,243	KIM, WOO-HYUN	
	Examiner	Art Unit	
	Phu Vu	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection necessitated by an amendment.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 and 5-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishiki US 5946060.

Regarding claims 1, Nishiki teaches a liquid crystal display panel, comprising: a plurality of gate lines (fig. 2A elements 1A and 1B) arranged along a first direction on a first substrate; a plurality of data lines (fig. 2B element 2) arranged along a second direction on the first substrate to cross the gate lines to define a plurality of unit pixels; an insulating layer (fig. 2B element 9) disposed over the gate and data lines; a common electrode (figs. 1A-1B element 5A) disposed on a second substrate opposite the first substrate; a plurality of pixel electrodes (4A) each pixel electrode provided in each of the unit pixels partitioned by the gate line and the data line; and a plurality of side electrodes (5B) overlapping the data lines along a length direction of the data lines, the side electrode in the pixel being extended to a neighboring pixel (see fig. 2A element 5B), wherein the insulating layer(9) is provided between the side electrode (5B) and

the data lines (2) and a width of the side electrode is greater than a width of the data lines.

Regarding claim 2, Nishiki teaches a TFT transistor provided in the unit pixel (fig. 3A element 3A).

Regarding claim 5, Nishiki teaches the side electrodes are provided between the adjacent unit pixels (see fig. 2B element 5B).

Regarding claim 6-7, Nishiki teaches the insulating layer including an organic material film of a photo-acryl (see column 3 line 42).

Regarding claim 8, Nishiki teaches the side electrodes overlap the gate liens with at least the insulating layer therebetween (see fig 2A elements 1A and 5b).

Regarding claim 9, the limitation "the pixel electrode is divided into a first region and a second region and the first and second regions are electrically interconnected by a connection region" is met by the reference as the limitation of divided and connection regions can be arbitrarily defined. For instance with respect to figure 2 the top part of element 4A can be considered a first region the bottom part can be considered the second region and the "connection region" can be considered the part overlapping 4b.

Regarding claim 10, Nishiki teaches a liquid crystal panel, comprising: a plurality of gate lines (fig. 3A element 1a) formed on a first substrate (fig. 3B element 6a); a first insulating layer (fig. 3B element 7) and an active layer (fig. 3A element 104a and 104b) formed on the first substrate; a plurality of data lines(fig. 3A element 2) on a surface of the active layer; a second insulating layer (figs. 5B element 9) formed on another surface of the active layer upon which the data lines are formed; a plurality of

side electrodes (fig. 2B element 5b) formed on a surface of the second insulating layer to overlap the data lines (2) along a length direction of the data lines the side electrode in the pixel being extended to a neighboring pixel; and a plurality of pixel electrodes (4b) formed on surfaces of the second insulating layer separated from the side electrodes (5b), wherein a width of the side electrode is greater than a width of the data lines.

Regarding claim 11, Nishiki teaches the first insulating layer is a gate-insulating layer separating a gate electrode from the active layer (see fig. 3B and 4B element 7). The gate electrode is considered to be the same layer as the gate lines.

Regarding claim 12, Nishiki teaches the second insulating layer including an organic layer (column 3 line 42).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiki in view of Kim US 5338240.

Regarding claims 3-4, Nishiki teaches all the limitations of claims 3-4 except forming the pixel and side electrodes of the same material and a transparent conductive film. Kim teaches ITO (a transparent conductive film) that can be patterned by conventional photolithography techniques (column 1 lines 48-55). Therefore, at the time

of the invention, it would have been obvious to one of ordinary skill in the art use ITO to enable patterning by conventional photolithography techniques.

Claim 13-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiki in view of Applicant's Admitted Prior Art (AAPA) in view of Kim US 5338240.

Regarding claims 13, 15-17 and 20, Nishiki teaches a second substrate bonded to the first substrate (fig. 1A and 1B element 6b), a liquid crystal material (15) formed between the first and second substrates; a black matrix (14) formed on a surface of the second substrate aligned to the gate lines and the data lines, a common electrode (5a) formed on another surface of the second substrate upon which the black matrix and the color filter (13) layer are formed. Nishiki fails to teach an electric field partition formed on the second substrate in the form of ribs formed on the surface of the common electrode or a slit formed and a plurality of partitions formed on the first substrate between adjacent ones of the plurality of pixel electrodes and wherein the liquid crystal layer has negative dielectric anisotropy. AAPA teaches an electric field partition formed on the second substrate in the form or ribs (see related art fig. 1 element 25), or a slit (see related art fig. 2 element 36) formed between adjacent portions of the common electrode with a liquid crystal layer having negative dielectric anisotropy ([0011]) that achieves improved contrast ratio and response time ([0013] and [0016-0020] and [0028]). Therefore, it would have been obvious to one of ordinary skill in the art to apply electric field partitions and a negative dielectric liquid crystal layer to improve contrast ration and response time. Nishiki and AAPA fail to teach the side electrodes, pixel

electrode made of a transparent conductive material including ITO however Kim teaches ITO as an electrode material that can be patterned with conventional photolithography techniques. Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to use ITO in order to allow for patterning by conventional photolithography techniques.

Regarding claim 14, Nishiki teaches a liquid crystal material formed between the first and second substrates (see fig. 1A and 1B).

Regarding claim 18, Nishiki teaches a plurality of electric field partitions a plurality of electric filed partitions formed on the first substrate between adjacent ones of the pixel electrodes (see figs 1A and 1B elements 4b and 5b).

Regarding claims 19 and 22-23, Nishiki teaches a method of fabricating a liquid crystal display panel comprising: forming a plurality of gate lines (fig. 2A elements 1A and 1B), a plurality of data lines (fig. 3A element 2), and a plurality of TFTs (fig. 3A element 3A) on a first substrate; forming a passivation layer (fig. 2B element 9) on a surface of the first substrate upon which the gate lines, the data lines, and the TFT transistors are formed; forming a transparent conductive material (4b) on a surface of the passivation layer; forming a plurality of side electrodes (5b) extending along a length direction of the data lines and overlapping the data lines by patterning the transparent conductive material, the side electrode in the pixel being extended to a neighboring pixel; forming a plurality of pixel electrodes (4b) separated from the side electrodes by patterning the transparent conductive material, forming a black matrix (figs 1A and 1B element 14), a color filter (fig. 1A-1B element 13), and a common electrode (fig. 1A – 1B

element 5a) on a second substrate; bonding the first and second substrates together aligning the pixel electrode to the common electrode (see fig. 1A or 1B); and forming a liquid crystal layer (fig. 1A or 1B element 15) between the bonded first and second substrates, wherein a width of the side electrode is greater than a width of the data lines (see element 5b and 2a). Nishiki fails to teach forming an electric field partition on the common electrode in the form of a rib or slit. APA teaches an electric field partition formed on the second substrate in the form or ribs (see related art fig. 1 element 25), or a slit (see related art fig. 2 element 36) formed between adjacent portions of the common electrode ([0011]) that achieves improved contrast ratio and response time ([0013] and [0016-0020] and [0028]). Therefore, it would have been obvious to one of ordinary skill in the art to apply electric field partitions of ribs or slits on the common electrode to improve contrast ratio and response time.

Regarding claim 21, Nishiki teaches etching the passivation layer to expose the drain electrode portions of the TFTs (see column lines "contact hole" contacting the drain electrode).

Regarding claim 24, Nishiki teaches a plurality of side electrodes and pixel electrodes (see claim 19 rejection) however the reference fails to teach these formed by patterning however AAPA discloses this process as known in the prior art to pattern the side electrode and pixel electrode (see [0028]). Processes known or conventional in the art have inherent limitation of usually lower cost and improved reliability. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to

simultaneously form the side and pixel electrodes by patterning to gain benefits of conventionality.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phu Vu whose telephone number is (571)-272-1562. The examiner can normally be reached on 8AM-5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571)-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phu Vu
AU 2871

ANDREW SCHECHTER
PRIMARY EXAMINER